Development of granular, fast and low power CMOS pixel sensors with intrinsic gain for charged particle detection

IPHC has been one of the precursors of the development of monolithic CMOS pixel sensors (MAPS), which have become an attractive tool to equip charged particle trackers for experiments like STAR, ALICE, Belle II, LHCb and FCCee. Their main advantage lies in the fact that the detection node, typically a reverse-biased diode, and the conditioning electronics are integrated on the same substrate. Thus, within each pixel there is a detecting node connected to its preamplifier, whose signal is then digitized for reading and processing by an embedded logic. Currently, the sensing node has no intrinsic amplification and the preamplifier must be carefully designed to meet requirements at the limits of the state of the art, especially when it comes to generating fast signals of a few tens of picoseconds despite a very constrained power budget. A solution is sought by increasing the intrinsic gain of the current collection diodes through a controlled avalanche. The resulting fast signals would allow to consider the direct drive of the digitization stage.
Such sensing nodes follow the approach of Low Gain Avalanche Diodes (LGAD) structures. But in contrast to LGAD which are not monolithic and have a low granularity (typically 1mm²), highly miniaturized (~200 µm²) pixels will be integrated thanks to the CMOS technology leading to a new MAPS generation featuring ultra-high performance.

After a bibliographical study on silicon avalanche detectors, the first step in this internship will be to characterize the foundry process already used at the IPHC. We will then ensure that it is suited for the design of new prototypes. For this, an experimental approach will be conducted, using MAPS prototypes already designed for charge collection with fine pixels at low speed. By applying a higher than usual voltage, it will be possible to enter the controlled avalanche regime. This will allow the student to become familiar with these physical phenomena. Preliminary evaluations have already shown promising signs.
The second part of the internship will focus on the study and design of a new pixel. The work will start with the study of pixel geometries. The aim will be to optimize by simulation the avalanche phenomenon created during the passage of a particle. This will be done using TCAD silicon structure modeling tools such as Synopsys Sentaurus. The student will then be able to follow the realization of a small pixel array under the responsibility of a senior microelectronics engineer.
The internship will be carried out at C4PI, a facility specialized in the R&D of integrated pixel CMOS sensors.
This work could be followed by a PhD thesis for which funding has already been secured.

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